REMARKS

The Office Action of 01/28/2005 has been carefully considered. Reconsideration of the present application is respectfully requested.

Claims 6-8 were rejected as being anticipated by Fuller in view of Yamahata. Claim 6 has been previously amended to more clearly distinguish over the cited reference.

A distinguishing feature of the present invention as set forth in claim 6 is the ability of a processor to itself control whether or not the processor's cache is bypassed, enabling the cache to be switched off for power savings. Note in particular the fourth element of claim 6, reciting "a cache-bypass mode-control signal input for said processor to indicate indicate a cache bypass mode in response to a programmer instruction inserted in a program being executed by said processor explicitly for the purpose of switching to cache bypass mode."

In Fuller, by contrast, the programmer does not have any such control. Rather, a power management unit, in response to a fixed control program, determines whether or not cache-bypass mode will be entered.

Furthermore, in Yamahata, cache-bypass mode is inferred from selected instructions as made clear in col. 2 thereof, i.e., IN or OUT instructions, STRING instructions, PRIVILEGE

instructions, TASK SWITCHING instructions, or SEMAPHORE DATA operation instructions. Such a mechanism remains inflexible compared with the claimed invention.

Accordingly, it is respectfully submitted that the pending application, with pending claims 6-8, is in condition for allowance and such action is respectfully requested.

Should the Examiner be of the opinion that a telephone conference with Applicant's attorney would expedite matters, the Examiner is invited to contact the undersigned.

Respectfully submitted,

Dated: April 28, 2005

By: _____
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Reg. 33,089